UNITED STATES PATENT AND TRADEMARK OFFICE

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10/673,506	09/30/2003	Eric J. Strang	231753US6YA	1663

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EXAMINER
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ART UNIT	PAPER NUMBER
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NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _19 May 2008_.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-62 and 66-68_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-62 and 66-68_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _3/17/08_.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   This office action is in response to application 10/673,506 and amendment with

notice of appeal filed on 5/19/2008. Claims 1-62, 66, 67 and 68 remain pending in the

application.

Terminal Disclaimer

2.   The terminal disclaimer filed on 5/19/08 disclaiming the terminal portion of any

patent granted on this application which would extend beyond the expiration date of any

patent issuing from application Serial No. 10/673,138; 10/673,467; 10/673,501;

10/673,507; and 10/673,583 has been reviewed and is accepted. The terminal

disclaimer has been recorded.

Claim Rejections - 35 USC § 101

3.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of
> matter, or any new and useful improvement thereof, may obtain a patent therefore, subject to the
> conditions and requirements of this title.

4.   Claim 66 is rejected under 35 U.S.C. 101 because the claimed invention is

directed to non-statutory subject matter. A computer readable medium as claimed may

include a carrier wave (see 0105 of the specification) which is non-statutory subject

matter because there is no physical structure. Recommend changing to "a physical

storage device" instead.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed
> or described as set forth in section 102 of this title, if the differences between the
> subject matter sought to be patented and the prior art are such that the subject
> matter as a whole would have been obvious at the time the invention was made
> to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was
> made

6.   Claims 1-25, 32-56 and 66-68 are rejected under 35 U.S.C. 103(a) as being

obvious over Sonderman et al. (6,802,045) in view of Kee et al. (5,583,780).

7.   As to claims 1, 32, and 66, Sonderman et al. teach substantially similar claimed

invention of a method and apparatus for analyzing a process performed by a

semiconductor processing tool (Fig. 1-8 and its description) comprising inputting

process data relating to an actual process performed by the semiconductor processing

tool (process control environment 180 receives process data (process data relating an

actual process being by semiconductor processing tool) from the manufacturing

environment 170, at least col. 3 lines 50-64; Fig. 1); inputting a first principles physical

model relating to the semiconductor tool (simulation environment 210 that includes

device physics model, process model and equipment model, at least see in col. 5 lines

10-67; Fig. 3); performing a first principles simulation for the actual process being

performed during performance of the actual process (col. 5 lines 10-67; col. 7 lines 1-

20) using the physical model to provide a first principles simulation result (simulation

data output by a simulator 340 of Fig. 3; at least col. 7 lines 37-62) in accordance with

the process data relating to the actual process being performed in order to simulate the

actual process being performed in order to simulate the actual process being performed

(col. 3 lines 50-63; col. 4 lines 48-64; col. 5 lines 10-40; col. 7 lines 4-20; Fig. 1-3, 5, 8;

col. 5-7; specifically Fig. 3 describes a simulator simulates device physics model to

provide a first principles simulation data result; the device physics model 310, the

process model 320 and the equipment model 330 perform the functions or conditions of

the device, process, and equipment, respectively, during a particular manufacturing

process, col. 5 lines 10-67; the process control environment 180 utilizes the simulation

data received from the simulation environment 210 in order to make control parameter

adjustment or modifications for controlling manufacturing processes, col. 5 lines 40-47;

the device physics model 310 comprises components that can measure electrical

characteristics of a semiconductor wafer being manufactured; the device physics model

comprises components that emulate or measure growth of oxide film on a

semiconductor wafer; the device physics model 310 comprises components that can

model the chemical reactions that can take place one a semiconductor wafer being

processed, the process model and equipment are described (col. 5 lines 47-55); and

using the first principles simulation result obtained during the performance of the actual

process to determine a fault (error) in the process performed by the semiconductor

processing tool (Fig. 1-8, col. 5-7; specifically the simulation environment 210 includes a

process control interface 350 allowing the simulation environment 210 to perform

feedback corrections during the manufacturing of semiconductor wafers, col. 5 lines 18-

27; the simulation environment 210 determines any error due to variations in the

components in the defined models; using this error data, the system 100 of Fig. 1

performs a predictive state analysis 750 and sensitivity analysis 760 of Fig. 7;

performing the predictive state analysis comprising predictive how a certain component

within one of the models 310, 320, 330 behaves in response to modifications to another

component in any one of the models in order to determine an optimum component

levels to be implemented during manufacturing processes, described in col. 8, lines 12-

67). Sonderman et al. also teach simulating process task (actual process) to provide

simulation data results to enhance manufacturing process (col. 6 lines 24-64).

Specifically, Sonderman et al. teach the simulation environment including the above

integrated physical model and process model that is simulated by a simulator (Fig. 3).

The teachings of the simulation environment that includes device physics model,

process model and equipment model (Fig. 3, col. 5 lines 10-18, lines 47-55), clearly

suggest that the models must include some equations that are used for computation in

order to determine electrical characteristics, growth of oxide film, control parameters

and temperature. Some of equations are described in column 9. Accordingly,

Examiner believes that the simulation environment that includes a physics model,

process model and equipment model correspond to physics-based first principles

model. The simulation environment comprises a process control interface that allows

communications between the simulation environment to receive manufacturing data

from the manufacturing environment which can be used by the simulation environment

to perform feedback corrections during the manufacturing of semiconductor wafers.

There is an interaction performance between these models (physical model, process

model and equipment model). Therefore, any modifications to any one of the three

models can be made and analyzed by the simulator. The process control environment

(item 180 Fig. 1) utilizes the simulation data received from the simulation environment in

order to make control parameter adjustments or modifications for controlling

manufacturing processes. The physics model comprises components that emulate or

measure growth of oxide film on a semiconductor wafer. The device physics model also

comprises components that can model the chemical reactions that can take place on a

semiconductor wafer being processed. The process model and equipment model are

described (col. 5 lines 47-67). Thus, Sonderman et al. do not teach the first principles

physical model including a set of computer-encoded **differential equations.** Kee et al.

teach modeling apparatus that include physical models including differential equation

that can be used to develop real-time control systems for a particular actual thermal

system for processing a silicon wafer using physically simulations (Fig. 1-2, see

summary; col. 3 lines 44-50; col. 4 lines 33-38; col. 5 lines 1517; col. 5 lines 36-45; col.

7 lines 1-10). The modeling apparatus (physical models) include a set of computer-

encoded differential equations of the physical model parameters to quickly account for

spectral-radiation effects used in design and real-time control systems (col. 7 lines 3-44;

col. 5 lines 23-67; col. 6 lines 1-67; col. 11 lines 14-67; col. 12 lines 1-67; Figs. 1-2).

Columns 7-10 describe set of differential equations. Thus, the modeling apparatus

includes set of differential equations (first principles physical model that includes set of

differential equations) can be used with confidence to predict effects of various

approximations in the radiation transport and to facilitate the design of actual thermal

systems (col. 12 lines 29-41). In addition, the modeling system with differential equation

executes quickly, even when processing unit 110 is implemented on workstation class

computing platform. Thus, the modeling apparatus/system 101 quickly accounts for

spectral-radiation effects, and, as described above, may used in design and real-time

control system for processing a semiconductor wafer (col. 7 lines 3-10; col. 5 lines 15-

17; col. 5 lines 36-45). With above expected results and motivation as described above,

integrating the differential equations as taught by Kee et al. in Sonderman's first

principles physical model would have been obvious to practitioners in the art at the time

the invention. The new added limitation, first principles simulation result being produced

in a time frame shorter in time than the actual process being performed is obvious to

artisan skill in the technological art. It is well known to artisan in the art that speed of

processor used to run simulation determines a time frame to produce a simulation result

(first principles simulation result as taught by Sonderman). Different speed of processor

is available. It is recognized to artisan skill in the art there is an advantage to obtain a

simulation result ready for the actual process being performed because the simulation

result is used to subsequently or sequentially or concurrently control process being

performed. For at least these reasons, the newly added claimed limitation is obvious to

artisan skill the art.

8.   As to claims 2 and 33, Sonderman et al. teach directly inputting the data (input

data, process, manufacturing data, input control parameters) relating to a process

performed by the semiconductor processing tool from at least on the physical sensor

and a metrology tool physically mounted on the semiconductor processing tool (Fig. 1,

7, col. 4-8).

9.   As to claims 3-5 and 34-36, Sonderman et al. teach indirectly inputting the data

relating to a process performed by the semiconductor processing tool from at least one

of a manual input device and a database, inputting data recorded from a process

previously performed by the semiconductor processing tool, inputting data set by a

simulation operator (Fig. 1-3, col. 1, manual fashion and automated fashion, col.4-7).

10.   As to claims 6-9 and 37-40, Sonderman et al. teach inputting data relating to at

least one of the physical characteristics of the semiconductor processing tool and the

semiconductor tool environment, data relating to at least one of a characteristic and a

result of a process performed by the semiconductor processing tool; inputting a spatially

resolved model of the geometry (modified models) of the semiconductor processing

tool; inputting fundamental equations necessary to perform first principles simulation for

a desired simulation result (Fig. 1-3, col. 5-9).

11.   As to claims 10-13 and 41-44, Sonderman et al. performing interaction

concurrently between simulation environment (first principles simulation) and the

semiconductor processing tool (Fig. 2); performing simulation environment (first

principles simulation) and the semiconductor processing tool (Fig. 2); performing first

principles simulation using the input data to set a boundary condition and an initial

condition of the first principles simulation model (Fig. 3, col. 5-8).

12.   As to claims 14 and 45, Sonderman et al. teach using the simulation result

(simulation data, simulation data result) to detect a fault in the process performed by the

semiconductor processing tool by comparing the first principles simulation result with

the input data (col. 7, Fig. 5-7).

13.   As to claims 15-19 and 46-50, Sonderman et al. teach a system having a

network of interconnected resources to perform at least one of the process steps as

recited in Claim 1; using code parallelization among interconnected computational

resources to share the computational load of the first principles simulation; sharing

simulation information among interconnected resources to determine the fault in the

process performed by the simulation processing tool; distributing simulation results

among the interconnected resources to reduce redundant execution of substantially

similar first principles simulations by different resources; distributing model changes

among the interconnected resources to redundant refinements of first principles

simulations by different resources (Fig. 1-3, computer code software is described in col.

9 starting line 58; col. 5-8).

14.   As to claims 20-21 and 51-52, Sonderman et al. teach remote access (Col. 9

line 58 to col. 10 line 31). Note that a wide area network is art inherent.

15.   As to claims 22 and 53, Sonderman et al. teach performing simulation utilizing a

computer software code (Col. 9 line 58 to col. 10 line 31).

16.   As to claims 23-25 and 54-56, Sonderman et al. teach using the first principles

simulation result (simulation data set results) to classify a fault in the process performed

by the semiconductor processing tool (col. 6, lines 1-35); calculating a set of

perturbations solutions corresponding to the first principles simulation for input data to

generate a profile data solutions to the first principles simulation, inputting the

perturbation solutions to a multivariate analysis; inputting a difference between the first

principles simulation result and the input data to the multivariate analysis; and utilizing

the multivariate analysis to identify a correlation between the input data and the

difference (defining variations into the components of defined models in order to

simulate the effects of online manufacturing performance by the models; modified

models) (col. 5-8).

17.   As to claims 67-68, the integrated physical model as taught by Sonderman et al.

and Kee et al. corresponds to a first principles physical model as claimed as described

in above rejection. The simulation environment included the above integrated physical

model is simulated by a simulator (Fig. 3 of Sonderman). The simulation environment

includes device physics model, process model and equipment model (Fig. 3, col. 5 lines

10-18). The simulation environment comprises a process control interface that allows

communications between simulation environment to receive manufacturing data from

the manufacturing environment which can be used by the simulation environment to

perform feedback corrections during the manufacturing of semiconductor wafers. There

is an interaction performance between these models (physical model, process model

and equipment model). Therefore, any modifications to any one of the three models

can be made and analyzed by the simulator. The process control environment (item 180

Fig. 1) utilizes the simulation data received from the simulation environment in order to

make control parameter adjustments or modifications for controlling manufacturing

processes. The physics model comprises components that emulate or measure growth

of oxide film on a semiconductor wafer. The device physics model also comprises

components that can model the chemical reactions that can take place on a

semiconductor wafer being processed. These teachings correspond to providing for the

first principles simulation a reuse of known solutions as initial conditions for the first

principles simulation because the simulation data is reused as initial conditions for the

simulation environment.

18.   Claims 26-31 and 57-62 are rejected under 35 U.S.C. 103(a) as being obvious

over Sonderman et al. (6,802,045) in view Kee et al. (5,583,780) in further view of Fatke

et al. (US 2005/0016947).

19.   As to claims 26-28 and 57-59, Sonderman et al. do not explicitly teach the

multivariate analysis comprising a partial least square analysis; defining a set of loading

coefficients, computing at least one of mean and standard deviation values. Fatke et al.

teach these limitations including defining a correlation matrix in order to improve

detection of a feature etch completion process during semiconductor manufacturing to

thereby providing accurate and precise completion of an etch process (see abstract,

Fig. 4, summary, 0051). Therefore, it would have obvious to one of ordinary skill in the

art at the time the invention was made to combine these teachings in to the system as

taught by Sonderman et al. in order to provide an accurate and precise completion of a

process during semiconductor manufacturing.

20.   As to claims 29-31 and 60-62, Sonderman et al. attributing the difference

between simulated results and input data to one input data using the correlation; using

the simulation result to detect a fault comprising detecting a fault (error) in at least one

of a material processing system, an etch system, a photoresist spin coating system, a

lithography system, a dielectric coating system, a deposit system, a rapid thermal

processing system for thermal annealing and a batch diffusion furnace (examples described in col. 4; detecting a fault in at least one of a chemical vapor deposition system and a physical vapor deposition system (col. 4, 6, 7, 8).

Remarks

21.   A notice of appeal filed on 5/19/08 is acknowledged.

22.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
Primary Examiner, Art Unit 2825